What is claimed is:

1. A liquid crystal display device with a multi-timing controller, comprising:

a liquid crystal display panel having a display standard corresponding to an arranged pixel;

an interface receiving a data inputted from the exterior thereof and a control signal corresponding to the display standard;

a timing controller for latching and outputting a data inputted from the interface, and for generating and outputting timing signals for driving the liquid crystal display panel from the control signal; and

a driving circuit for receiving the timing signals from the timing controller to display a picture corresponding to the data on the liquid crystal display panel,

wherein said timing controller includes a display standard set part for setting one display standard in response to a plurality of display standards and generating a setting signal corresponding to the display standard, a selector having each timing generation information according the plurality of timing standards and outputting a timing information corresponding to the set signal, and a timing generator for receiving the timing information to generate and output the timing signals from the control signal.

2. The liquid crystal display device as claimed in claim 1, wherein the display standard set part sets any one of SVGA, XGA, SXGA, UXGA and VGA display standards using a dip switch.

3. The liquid crystal display device as claimed in claim 1, wherein the selector consists of a memory for storing a certain timing information and a multiplexor for selecting any one of the timing information stored in the memory.

4. The liquid crystal display device as claimed in claim 1, wherein the timing generator includes:

a first controller for generating the timing signal corresponding to the timing information selected from the selector;

a second controller for generating a liquid crystal polarity inversion signal indicating a driving voltage polarity of the liquid crystal provided on the liquid crystal display panel and a gate drive starting signal for notifying a first drive line of a field from one vertical synchronizing signal;

a third controller for generating a signal informing a sampling start of a data and a source sampling clock for latching a data at the rising or falling edge during one horizontal synchronization period;

a fourth controller for deforming a gate output enable signal generated from the first controller by making the gate output enable signal into a high state during a certain time so as to prevent a latch-up badness in which all the outputs of a gate drive integrate circuit goes to a high state, thereby disabling the gate drive integrated circuit; and

a fifth controller for always equally keeping the polarity of the horizontal/vertical synchronizing signal.

5. The liquid crystal display device as claimed in claim 4, wherein the first controller includes:

a first counter for receiving the horizontal

synchronizing signal inputted from the fifth controller and the first timing information inputted from the selector to count the timing information during two horizontal periods and thus output a first count value;

a subtractor for subtracting the timing information from the first count value to output a reference timing signal;

a second counter for counting the timing information every period of the horizontal synchronizing signal to output a second count value for the current horizontal period;

a first comparator for comparing the second count value with the reference timing signal to output a first selection timing signal;

a third counter for receiving the first selection timing signal as an initializing signal to count the reference clock during one horizontal period and thus output a third count value;

a second comparator for receiving the third count value to compare it with a second timing information inputted from the selector, thereby outputting a second selection timing signal when the two input values are equal;

a third comparator for receiving the third count value to compare it with a third timing information inputted from the selector, thereby outputting a third selection timing signal when the two input values are equal;

a fourth comparator for comparing the second count value with a fourth timing information inputted from the selector to output a fourth selection timing signal when the two input values are equal;

a fifth comparator for comparing the second count

value with a fifth timing information inputted from the selector to output a fifth selection timing signal when the two input values are equal; and

a sixth comparator for comparing the second count value with a sixth timing information inputted from the selector to output a sixth reference timing signal when the two input values are equal.